A PHASE-ERROR SUPPRESSOR AND A METHOD OF SUPPRESSING PHASE-ERROR

ABSTRACT OF THE DISCLOSURE

The present invention provides a phase-error suppressor for use with a plurality of transistors having a common source coupled to a current generator that receives signals at a frequency. In one embodiment, the phase-error suppressor includes an inductor, coupled between the common source and the current generator, that resonates proportionally to the frequency with a first capacitance associated with the plurality of transistors. In one embodiment, the inductor resonates at about twice the frequency wherein input phase error is suppressed at output.